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Substitute for form 1449A/PTO				Complete If Known	
				Application Number	10/705,504
				Filing Date	November 10, 2003
				First Named Inventor	Leo Mathew et al.
				Group Art Unit	-Unassigned- 2818
				Examiner Name	Unassigned
Sheet	1	of	1	Attorney Docket Number	SC13161TP

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
TH	B1	SINGER, Pete; "Dual Gate Control Provides Threshold Voltage Options"; Semiconductor International; November 1, 2003; 2pp; URL http://www.reed-electronics.com/semiconductor/index.asp?layout=article&articleId=CA331000&text=motorola&rid=0&rme=0&cfid=1	

Examiner Signature	TH-THE + CO	Date Considered	Aug 2004
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¹ Unique citation designation number. ² Applicant is to place a check mark here if English Language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT			Application Number		
(use as many sheets as necessary)			Filing Date		
Sheet	1	of	Examiner Name	Leo Mathew et al.	<i>2818</i>
			Group Art Unit	Unassigned	
			Attorney Docket Number	SC13161TP	
U. S. PATENT DOCUMENTS					

Examiner Initials ¹	Cite No. ²	Document Number Number -Kind Code ³ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
TTP	A-1	US - 6,583,469	06-24-2003	Fried et al.	
	A-2	US - 2003/113970 A1	06-19-2003	Fried et al.	
	A-3	US - 6,472,258	10-29-2002	Adkisson et al.	
	A-4	US - 6,458,662	10-01-2002	Yu	
	A-5	US - 6,433,609	08-13-2002	Voldman	
	A-6	US - 6,414,356	07-02-2002	Forbes et al.	
	A-7	US - 6,413,802	07-02-2002	Hu et al.	
	A-8	US - 6,396,108	05-28-2002	Krivokapic et al.	
	A-9	US - 6,372,559	04-16-2002	Crowder et al.	
	A-10	US - 6,355,961	03-12-2002	Forbes	
	A-11	US - 6,330,184	12-11-2001	White et al.	
	A-12	US - 6,300,182	10-09-2001	Yu	
	A-13	US - 6,097,065	08-01-2000	Forbes et al.	
	A-14	US - 6,150,687	11-21-2000	Noble et al.	
	A-15	US - 6,011,725	01-04-2000	Eitan	
	A-16	US - 5,804,848	09-08-1998	Mukai	
	A-17	US - 5,689,127	11-18-1997	Chu et al.	
TTP	A-18	US - 4,859,623	08-22-1989	Busta	
		US -			
		US -			

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(use as many sheets as necessary)		Sheet	2	of	3

NON PATENT LITERATURE DOCUMENTS

Examiner Initials'	Cite No.'	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
TH	A-21	Related Application 10/074,732 entitled "Method of Forming a Vertical Double Gate Semiconductor Device and Structure Thereof" filed September 3, 2002 entitled
	A-22	Related Application 10/443,375 entitled "Transistor With Independent Gate Structures" filed May 22, 2003
	A-23	Related Application 10/443,908 "Memory with Charge Storage Locations" entitled filed May 22, 2003
TH	A-24	Related Application 10/427,141 entitled "Semiconductor Fabrication Process with Asymmetrical Conductive Spacers" filed April 30, 2003
TH	A-25	LEE et al.; "Multilevel Vertical-Channel SONOS Nonvolatile Memory on SOI"; IEEE Electron Device Letters, 2002; pp 1-3 and 208-209.
TH	A-26	YU, BIN et al; "FinFET Scaling to 10nm Gate Length"; IEEE IDEM 2002; pp 251-254; IEEE

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(use as many sheets as necessary) Sheet 3 of 3			Attorney Docket Number	SC13161TP	

NON PATENT LITERATURE DOCUMENTS (CONT.)					
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TH	A-27	CHOI, YANG-KYU et al.; "Sub-20nm CMOS FinFET Technologies"; 2001 IEEE, 4 pp..			
	A-28	KEDZIERSKI, JAKUB et al.; "High-Performance Symmetric-Gate and CMOS-Compatible VI Asymmetric-Gate FinFET Devices"; 2001; IEEE; 4 pp.			
	A-28	HISAMOTO, DIGH et al.; "FinFET – A Self-Aligned Double-Gate MOSFET Scalable to 20 nm"; IEEE Transactions on Electron Devices; Vol. 47, No. 12, December 2000, pp 2320-2325.			
	A-30	TANAKA, TETSU et al.; "Ultrafast Operation of V _{th} -Adjusted P+P Double Gate SOI MOSFET's; IEEE Electron Device Letters, Vol 15, No. 10, October 1994; pgs 386-388.			
	A-31	CHAN et al.; "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device"; IEEE Electron Device Letters; March 1987; pp 93-95; Vol. EDL-8, No. 3.			
	A-32	GONZALEZ, FERNANDO Sr. et al.; "A Dynamic Source-Drain Extension (DSDE) MOSFET Using a Separately Biased Conductive Spacer"; pp 645-648			
	A-33	KIM, KEUNWOO et al.; "Double-Gate CMOS Symmetrical – Versus Asymmetrical-Gate Devices"; IEEE Transactions On Electron Devices, Vol 48, No. 2; February 2001; pp 294-299.			
TH	A-34	FOSSUM, JERRY G. et al.; "Extraordinarily High Drive currents in Asymmetrical Double-Gate MOSFETS"; Superlattices and Microstructures, Vol 28, No. 5/6, 2000, 2000 Academic Press, pp 525-530.			

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